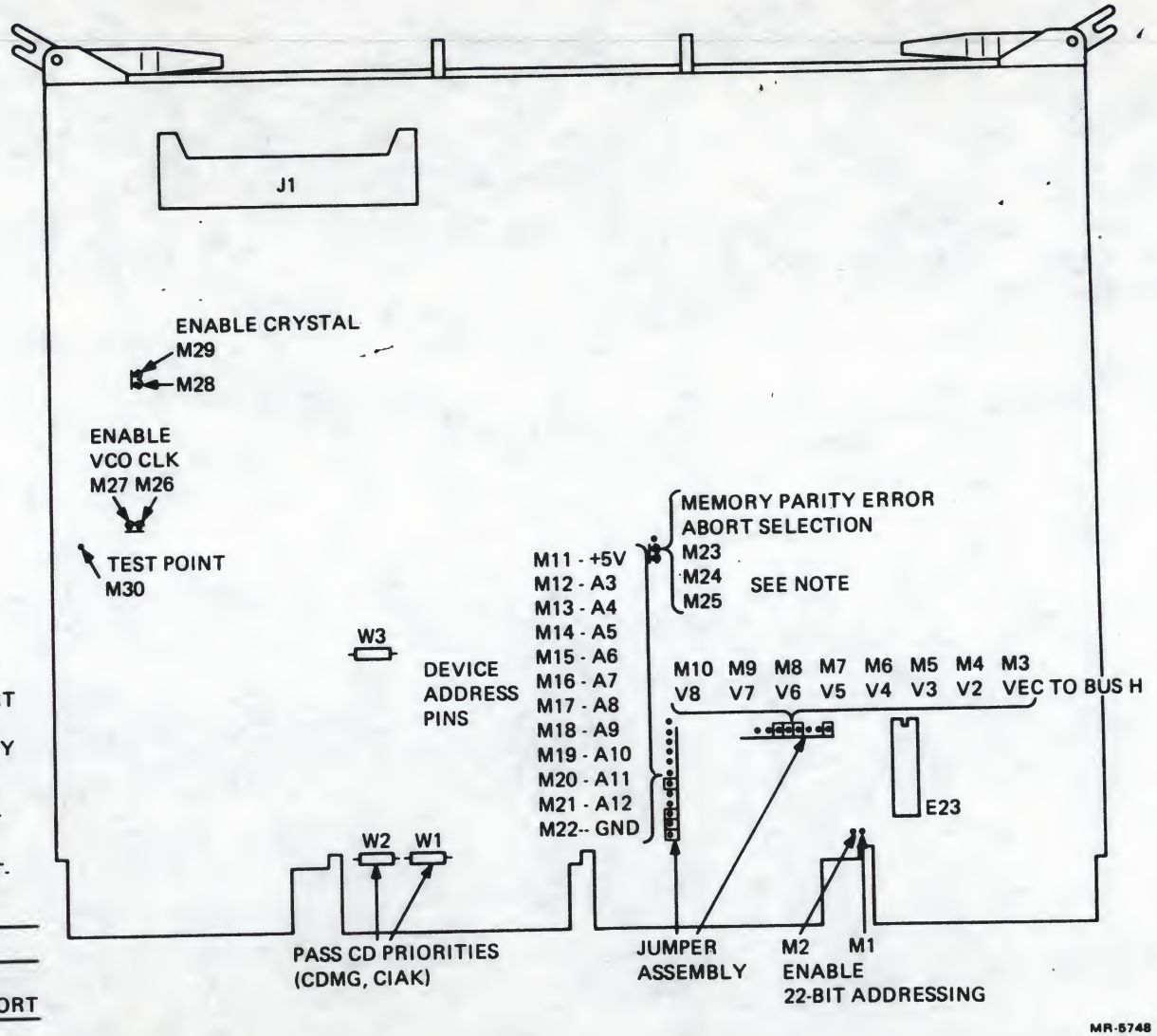
RLV12



NOTE:
THE MEMORY PARITY ERROR ABORT FEATURE IS AVAILABLE FOR USE WITH MEMORIES THAT HAVE PARITY ERROR CHECKING.
THIS FEATURE DOES NOT HAVE TO BE DISABLED FOR MEMORIES THAT DO NOT HAVE PARITY ERROR CHECKING. THE PINS ARE CONNECTED AS FOLLOWS:

CONNECTION	FUNCTION
M23 - M24	NO PARITY
M24 - M25	PARITY ERROR ABORT

Figure B-18 RLV12 Jumper Locations

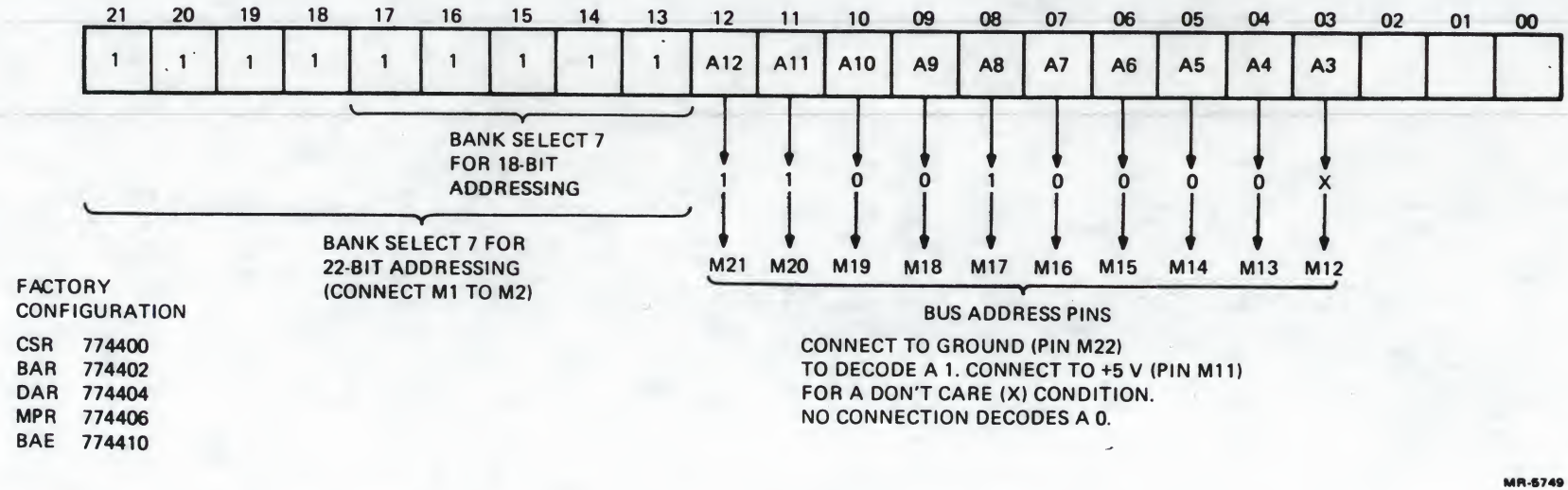


Figure B-19 RLV12 Device Address Format

NOTE

For 22-bit addressing, bit A3 is not decoded in the starting address.

B.6.3 Bus Selection

The RLV12 module can be used on 16-, 18-, or 22-bit LSI-11 buses. When sent from the factory, the module operates on 16- or 18-bit buses. To enable the module to operate on a 22-bit extended LSI-11 bus, install jumper M1 to M2, shown in Figure B-18. When installed, the jumper enables bank select 7 (BBS7) to be determined by the upper address bits (13–21). When the jumper is removed, the RLV12 has an 18-bit mode bank select 7 and can replace an existing RLV11 or RLV21 as the disk controller for RL01 and RL02 disk drives.

B.6.4 Interrupt Vector

The interrupt vector has a range of 0 to 774. The interrupt vector is preset at the factory to 160. The user may select another vector by changing the jumpers for bits V2–V8, as shown in Figure B-20. A connection to VEC TO BUS H (M3, shown in Figure B-18) generates a **1** for that bit; no connection generates a **0**.

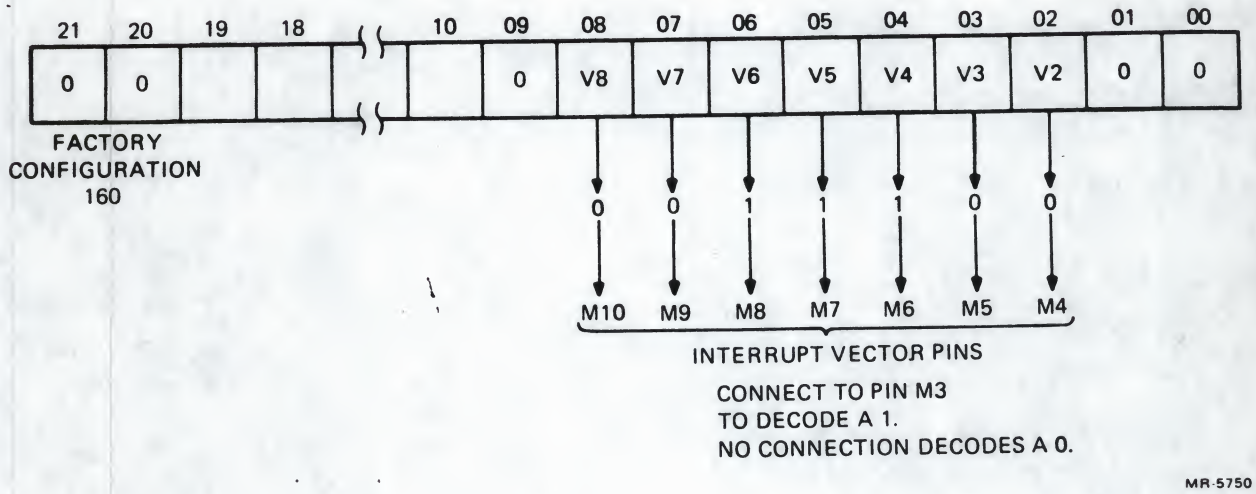


Figure B-20 RLV12 Format Interrupt Vector

B.6.5 Interrupt Request Level

The RLV12 interrupts at priority level 4 determined by the interrupt chip E23, a DC003.

B.6.6 Memory Parity Error Abort Feature

When reading the system's optional memory with parity error detection, a parity error will set OPI and NXM of the CSR. This is a unique error condition that aborts the current command to the RLV12. This error abort feature is possible only with memories that have parity data bits.

The RLV12 is sent from the factory with the memory parity error abort feature enabled. To disable parity error abort, remove the jumper between pins M24 and M25 and install a jumper between pins M23 and M24 (see Figure B-18). This feature does not have to be disabled for non-parity memories, as parity errors are not generated. Parity error abort uses data bits 16 and 17.

B.6.7 Other Jumpers

The module has two jumpers, W1 and W2, that enable priority signals to pass on the CD side of the module. The module has these jumpers installed and they should be left in when this controller is installed on the normal LSI-11 bus. If the RLV12 is installed in a C-D interconnect backplane with another module already in place, then these jumpers are removed. If the other module does not use the C-D interconnect scheme, then the status of jumpers W1 and W2 is not important.

Jumper	Signal
W1	CIAKI to CIAKO
W2	CDMG1 to CDMGO

One jumper, W3, enables the word count register to automatically increment during a DMA operation. This jumper is used for factory testing and should be left in.

Two jumpers on the module disable the crystal oscillator and the voltage-controlled oscillator during factory testing. These jumpers should be left in.

Jumper	Oscillator
M26-M27	VCO
M28-M29	Crystal

B.6.8 Installation

The RLV12 can be installed in any quad LSI-11 bus slot. The controller's priority level is based on its electrical distance from the processor module. Use the following procedure to install the module.

1. Examine the module to make sure that the base address jumpers and vector address jumpers are set correctly. (See Paragraphs B.6.2 and B.6.4.)
2. Check jumpers M1 and M2 for enabling the correct bank select 7 (BBS7) for the 18- or 22-bit LSI-11 bus.
3. If desired, disable the memory parity error abort feature. This feature can only be used with system memories that have parity options, but this feature does not have to be disabled for non-parity memories. (See Paragraph B.6.6.)
4. Insert the BC80M controller cable into J1 on the M8061.
5. Insert the M8061 in the selected slot in the LSI-11 bus.
6. Connect the other end of the BC80M cable to the drive.
7. Continue with the disk installation. (Refer to Paragraph B.8.)

B.6.9 Acceptance Testing

The RLV12 controller is tested by running the RLV12 diskless diagnostic test and, if a drive is attached, by running the diagnostics that exercise the RL01 and RL02 disk drive. The diskless diagnostic should be run first. The RLV12 diagnostics are available on different media. Contact your local DIGITAL sales office for the types of media available and their part numbers.

Run the XXDP+ diagnostics in the following order.

1. CVRLB RLV12 Diskless Diagnostic (16-, 18-, or 22-bit mode)
2. CZRLG Controller Test Part 1
3. CZRLH Controller Test Part 2
4. CXRLI Drive Test Part 1
5. CZRLJ Drive Test Part 2
6. CZRLN Drive Test Part 3
7. CZRLK Performance Exerciser
8. CZRLL Compatibility Test
9. CZRLM Bad Sector File Utility

NOTE

The Bad Sector File Utility is not a diagnostic test. It is used by Field Service personnel to examine the bad sector file on the disk and to write entries into that file.

B.7 RL8A CONTROLLER INSTALLATION

B.7.1 Introduction

The RL8A Omnibus controller module (M8433) contains the logic functions listed below.

- Interface logic
- Programmable registers
- Silo data storage and control
- Data formatting and error detection
- Control microsequencer and timing logic
- Drive bus interface logic

NOTE

Adjustments on the RL8A are preset at the factory and are not to be changed in the field.

B.7.2 Module Slot Location

The module can be inserted into any unused OMNIBUS hex-height slot between the CPU and the first memory element. The controller is connected to the first drive via a BC80J-20 interface cable. Connections between drives are made using a BC20J-XX (70-12122-10) cable.

B.7.3 Module Installation

1. Remove the M8433 module (see Figure B-18) and interface cable (BC80J-20) from the shipping container and inspect them for physical damage.

2. Verify the proper jumper configuration for device codes and priority (Figure B-21).

RLV12 DISK CONTROLLER

INTRODUCTION

The RLV12 disk controller interfaces RL02 and RL01 disk drives to any quad-or hex-size backplane that uses 16-, 18-, or 22-bit LSI-11 bus. One RLV12 controls up to four disk drives. The RLV12 consists of one quad-size module, a BC80M cable, a drive terminator, and drive identification hardware.

The RL01 and the RL02 are random-access, mass storage subsystems that store data in fixed-length blocks on a preformatted disk cartridge. Each RL01 can store 5.24 million bytes, and each RL02 can store 10.48 million bytes. The drives are 26.67 cm (10.5 in) high, self-cooling rack-mountable units and come complete with a power supply. Option RLV12-AK includes one RL01 drive, and option RLV22-AK includes one RL02 drive.

The RLV12 transfers data to and from the LSI-11 bus using Direct Memory Access (DMA) transactions. This allows data transfers to occur without processor intervention.

FEATURES

- Single quad-size module; needs no C-D connections
- Supports DMA data transfers in 16-, 18-, or 22-bit addressing modes
- Software-compatible with RLV11 controller (16-, or 18-bit modes only)
- Supports 22-bit addressing on an LSI-11 bus
- Controls from one to four RL01 and RL02 disk drives
- Memory parity error abort feature for use with memories that have a parity option

SPECIFICATIONS

RLV12 Disk Controller

Identification	M8061
Size	Quad-height: 26.56 cm × 1.27 cm × 22.70 cm (10.45 in × 0.5 in × 8.94 in)
Power requirements	+5 Vdc ± 5% at 5.0 A and +12 Vdc ± 5% at 0.1 A

Bus loads	
ac	3
dc	1
Addressing modes	16-, 18-, or 22-bit (determined by the user)
Max. config. for 22-bit address mode	H9275-A or similar backplane that supports 22-bit addressing, with memory capable of 22-bit addresses, such as the MSV11-L or the MSV11-P.
Limitations	The RLV12 will not fit in the dual-height LSI-11 mini-series H9281 backplane.
Drives per controller	Up to four RL01 and RL02 drives in any combination
LSI-11 addressable registers	8 (5 are used; 3 are not used)

Addressing Mode	Base Device Address
16-bit	17440_8
18-bit	774400_8
22-bit	17774400_8

Device interrupt vector	000160_8, jumper-selectable
Data transfer rates	4.9μs/word (avg) drive to controller, controller to memory I3.9μs/word (peak) drive to controller 2.0μs/word (peak) controller to memory
Error detection capability	Cyclic redundancy check (CRC) on data and headers. Memory parity error abort for use with memories that have parity checking.
Max. cable length (controller to last drive)	30 m(100ft)

)evice Address Selection

Software control of the RLV12 is performed by four or five device registers: CSR, BAR, DAR, MPR, and BAE. Four registers are used for 16- or 18-bit addressing; five registers are used for 22-bit addressing. The bus address extension register (BAE) is added for upper address but selection for 22-bit addressing. The usual device starting address is as follows:

Addressing Modes	Starting Address (Octal)
16-bit	174400
18-bit	774400*
22-bit	17774400

Factory configuration

NOTE

For 22-bit addressing, bit A3 is not decoded in the starting address.

The first register, the CSR, is assigned to the starting address, and the other registers are assigned to the next sequential address, as shown in Table 1.

The device starting address is selected by jumpers for bits 3-12. These jumpers are shown in Figure 1. A jumper from the selected bit to ground (M22) decodes a 1; no jumper decodes a 0; and a jumper to 5 V (M11) decodes an X (don't care) condition. Figure 2 shows the RLV12 device starting address format.

Bus Selection

The RLV12 module can be used on 16-, 18-, or 22-bit LSI-11 buses. When sent from the factory, the module operates on a 16-, 18-bit buses. To enable the module to operate on a 22-bit bus, install jumper M1 to M2, shown in Figure 1. When installed, the jumper enables bank select 7 (BBS7) to be determined by the upper address bits (13-21). When the jumper is removedthe RLV12 has an 18-bit mode bank select 7 and can replace an existing RLV11 or RLV21 as the disk controller for RL01 and RL02 disk drives.

Interrupt Vector

The interrupt vector has a range of 0 to 774. The interrupt vector is preset at the factory to 160. The user may select another vector by

changing the jumpers for bits V2-V8, as illustrated in Figure 3. A connection to VEC to BUS H (M3, shown in Figure 1) generates a 1 for that bit; no connection generates a 0.

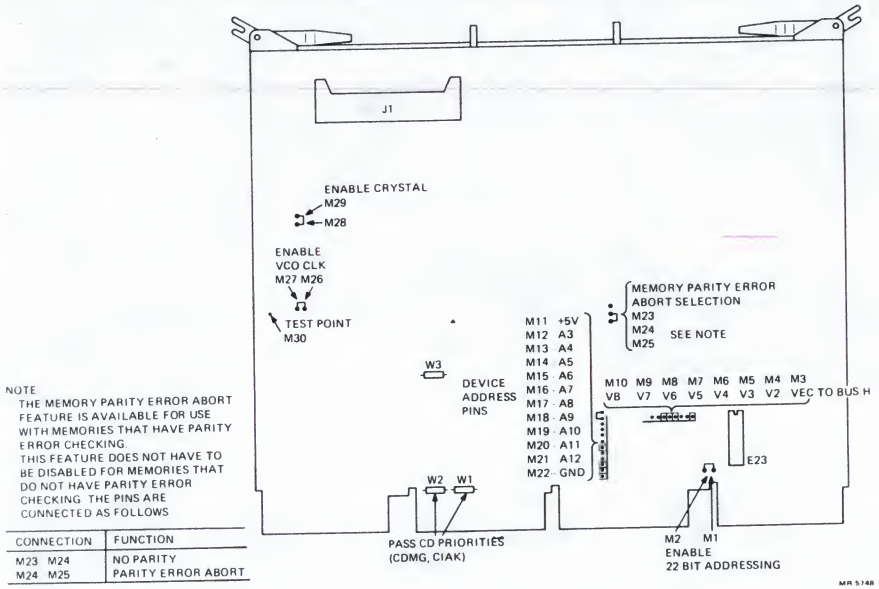
Interrupt Request Level

The RLV12 interrupts a priority level 4 determined by the interrupt chip E23, a DC003.

Table 1 Address Selection

Device Address	16-Bit Addressing	18-Bit Addressing*	22-Bit Addressing
Starting Address Range	160000–177770	760000–777770	17760000–17777760
Starting Address	174400	774400	17774400
No. of Registers	4	4	8 (5 are used; 3 are not)
Registers Used	CSR (174400) BAR (174402) DAR (174404) MPR (174406)	CSR (774400) BAR (774402) DAR (774404) MPR (774406)	CSR (17774400) BAR (17774402) DAR (17774404) MPR (17774406) BAE (17774410)
Jumpers Used	Tie M22 ("1") to M17, M20, and M21	Tie M22 ("1") to M17, M20, and M21	Tie M22 ("1") to M17, M20, and M21; Tie M11 ("X") to M12
Interrupt Vector			
Vector Range	0–774	0–774	0–774
Standard Vector	160	160	160
Jumpers Used	Tie M3 ("1") to M6, M7, and M8	Tie M3 ("1") to M6, M7, and M8	Tie M3 ("1") to M6, M7, and M8

*Factory Configuration



NOTE
THE MEMORY PARITY ERROR ABORT FEATURE IS AVAILABLE FOR USE WITH MEMORIES THAT HAVE PARITY ERROR CHECKING. THIS FEATURE DOES NOT HAVE TO BE DISABLED FOR MEMORIES THAT DO NOT HAVE PARITY ERROR CHECKING. THE PINS ARE CONNECTED AS FOLLOWS

CONNECTION	FUNCTION
M23 M24	NO PARITY
M24 M25	PARITY ERROR ABORT

Figure 1 RLV12 Jumper Locations

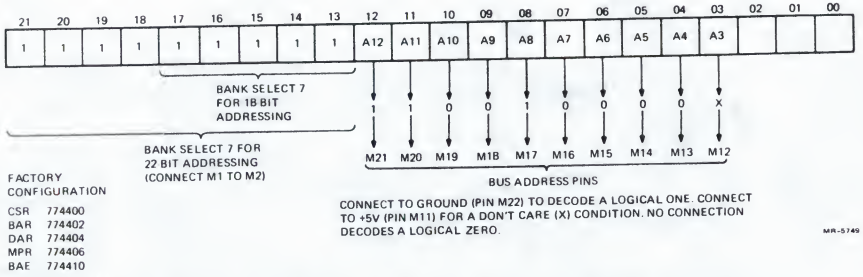


Figure 2 RLV12 Device Address Format

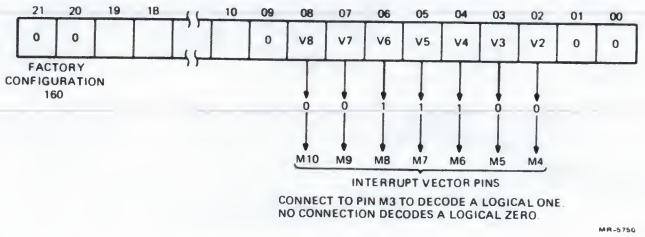


Figure 3 RLV12 Interrupt Vector Format

Memory Parity Error Abort Feature

When reading the system's optional memory with parity error detection, a parity error will set OPI and NXM of the CSR. This is a unique error condition that aborts the current command to the RLV12. This error abort feature is possible only with memories that have parity data bits.

The RLV12 is sent from the factory with the memory parity error abort feature enabled. To disable the parity error abort, remove the jumper between pins M24 and M25 and install a jumper between pins M23 and M24. (See Figure 1.) This feature does not have to be disabled for non-parity memories, as parity errors are not generated. Parity error abort uses data bits 16 and 17.

Jumpers That Remain Installed

The module has two jumpers, W1 and W2, that enable priority signals to pass through the module. The module has these jumpers installed, and they should be left in.

Jumper	Signal
W1	CIAKI to CIAKO
W2	CDMGI to CDMGO

One jumper, the W3, enables the word count register to automatically increment during a DMA operation. This jumper is used for factory testing and should be left in.

Two jumpers on the module disable the crystal oscillator and the voltage-controlled oscillator (VCO) during factory testing. These jumpers should be left in.

Jumper	Oscillator
M26-M27	VCO
M28-M29	Crystal

INSTALLATION

The RLV12 can be installed in any quad LSI-11 bus slot. The controller's priority level is based on its electrical distance from the processor module. Use the following procedure to install the module.

1. Examine the module to make sure that the base address jumpers and vector address jumpers are set correctly.
2. Check jumpers M1 and M2 for enabling the correct bank select 7 (BBS7) for the 18- or 22-bit LSI-11 bus.
3. If desired, disable the memory parity error abort feature. This feature can only be used with system memories that have parity options, but this feature does not have to be disabled for non-parity memories.
4. Insert the BC80M controller cable (or equivalent) into J1 on the M8061 as shown in Figure 4.
5. Insert the M8061 in the selected slot in the LSI-11 bus.
6. Attach the ground strap on the cable to the metal cabinet chassis.
7. Connect the other end to the BC80M cable to the back of the first disk drive.
8. Continue with the disk installation. Refer to the RL01/RL02 Disk Subsystem User Guide (EK-RL012-UG).

Acceptance Testing

The RLV12 controller is tested by running the RLV12 diskless diagnostic test, and, if a drive is attached, by running the diagnostics that exercise the RL01 and RL02 disk drive. The diskless diagnostic should be run first. The RLV12 diagnostics are available on different media. Contact your local DIGITAL sales office for the types of media available and their part numbers.

Run the XXDP + diagnostics in the following order:

1. CVRLB RLV12 Diskless Diagnostic (16-, 18-, or 22-bit mode)

NOTE

When the RLV12 is configured for 16- or 18-bit addressing, the RLV11 diskless diagnostic (CVRLA) is compatable with the RLV12 diskless diagnostic and checks the same logic.

2. CZRLG Controller Test, Part 1
3. CZRLG Controller Test, Part 1
4. CZRLH Controller Test, Part 2
5. CZRLI Drive Test, Part 1
6. CZRLJ Drive Test, Part 2
7. CZRLN Drive Test, Part 3
8. CZRLK Performance Exerciser
9. CZRLL Compatibility Test
10. CZRLM Bad Sector File Utility

NOTE

The bad sector file Utility is not a diagnostic test. It is used by field service to examine the bad sector file on the disk and to write entries into that file.